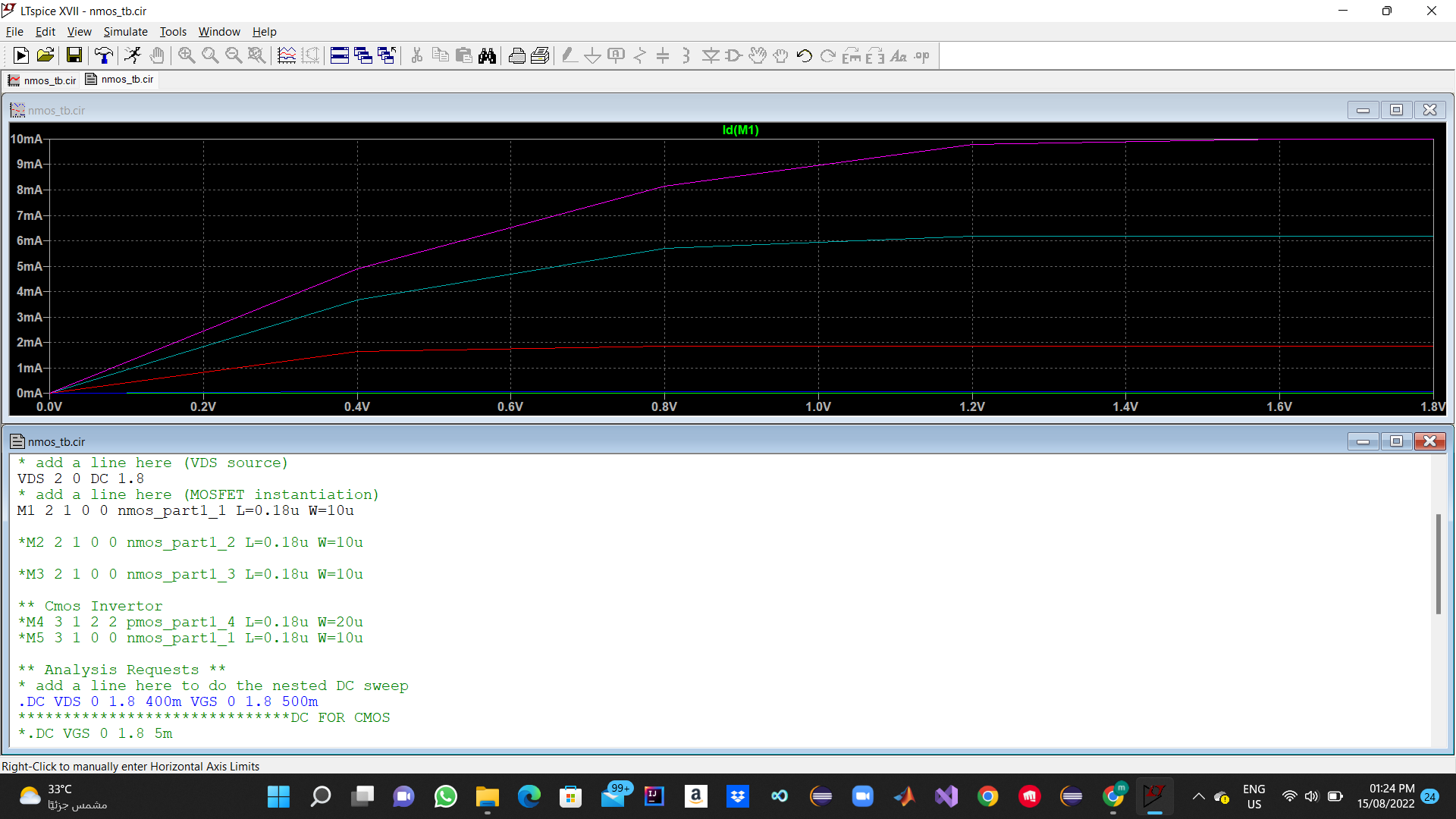
PART1:

**Question 1:**

ID Vs VDS with different vgs .(DC SWEEP)

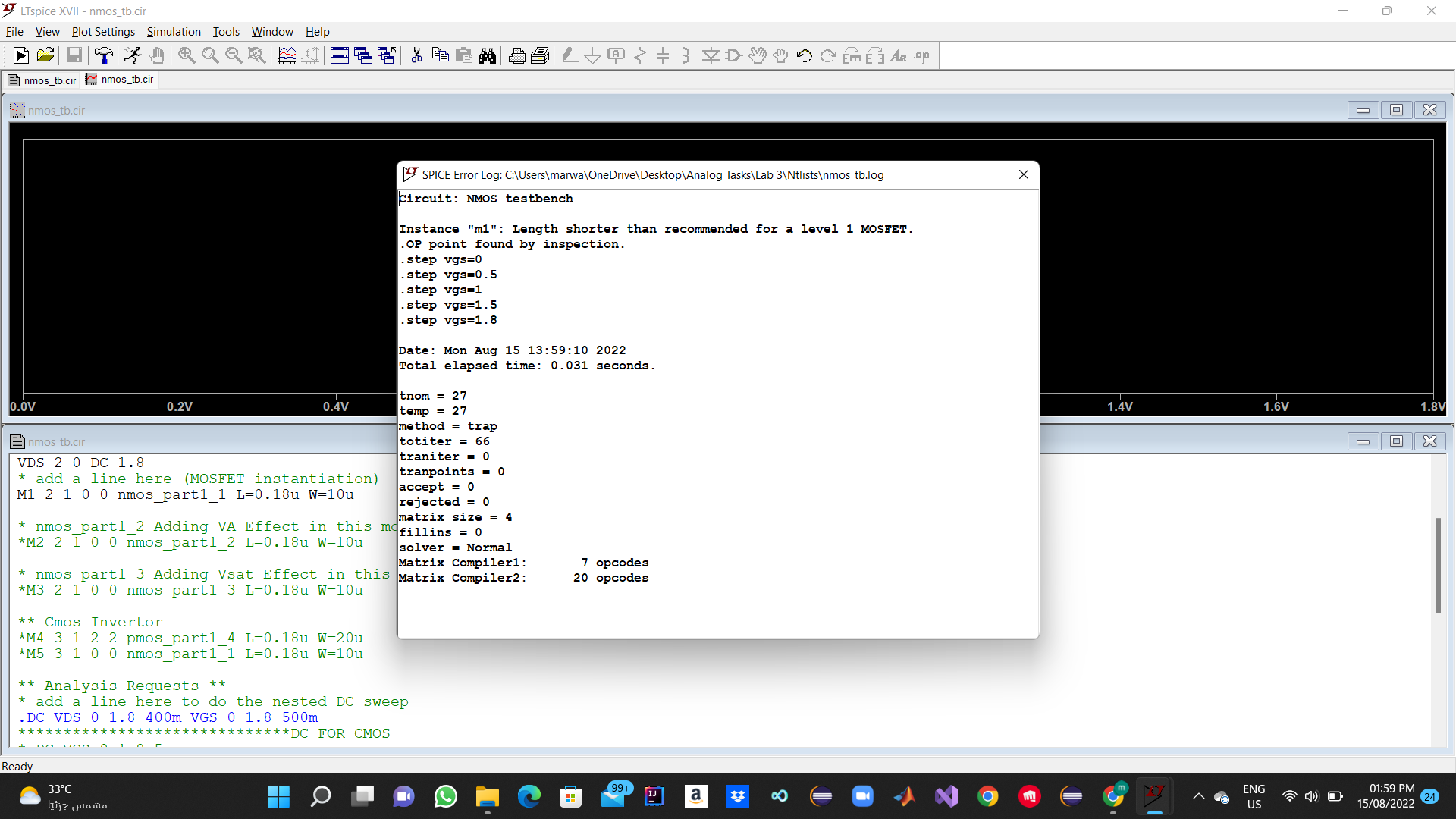


Nmos Model Used :

Graphical user interface, text, application

Description automatically generated

The Spice Error log Doesn’t recommend using Level 1 Model With This length it may be not Accurate (due to Short Channel Effect),



**Question 2:**

**Added Early Effect (Ro Effect) you can See slope at the saturation region .**

**Graphical user interface

Description automatically generated**

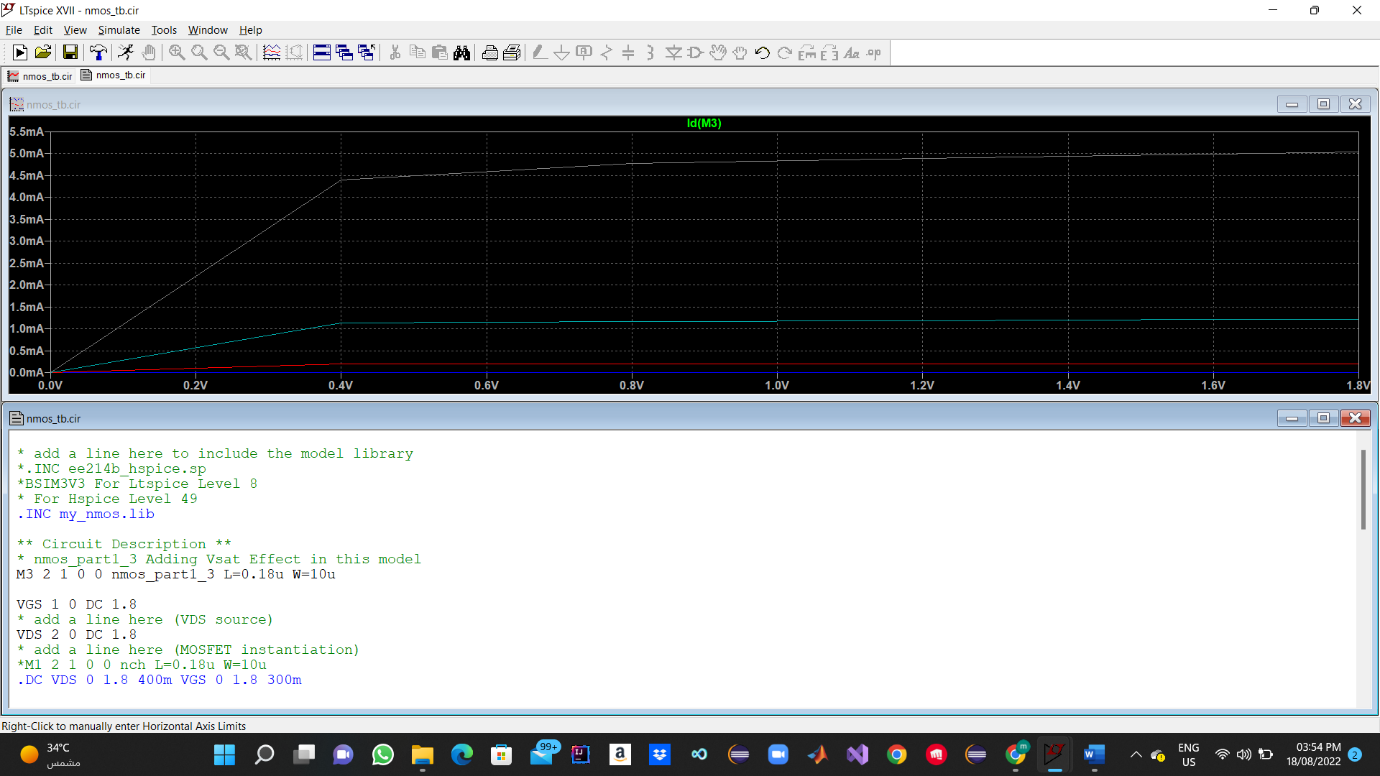
**Model Used :**

**Graphical user interface, text, application

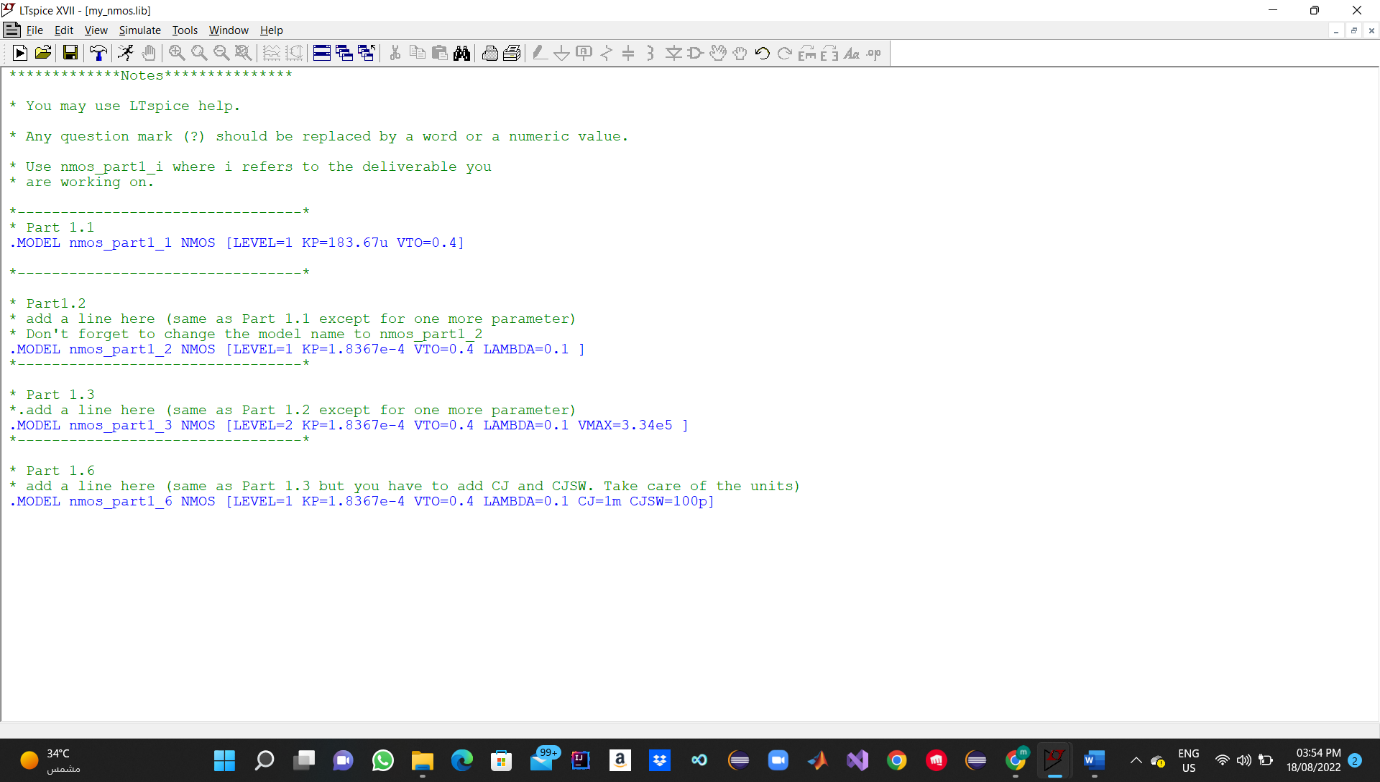
Description automatically generated**

**Question 3:**

**Velocity Saturation Effect Added.**

****

**Model Used :**

****

**Question 4:**

Vth must be -ve value (Pmos).

**Cmos Invertor Dc Characteristics**

A screenshot of a computer

Description automatically generated with medium confidence

**Cmos Invertor Netlists**

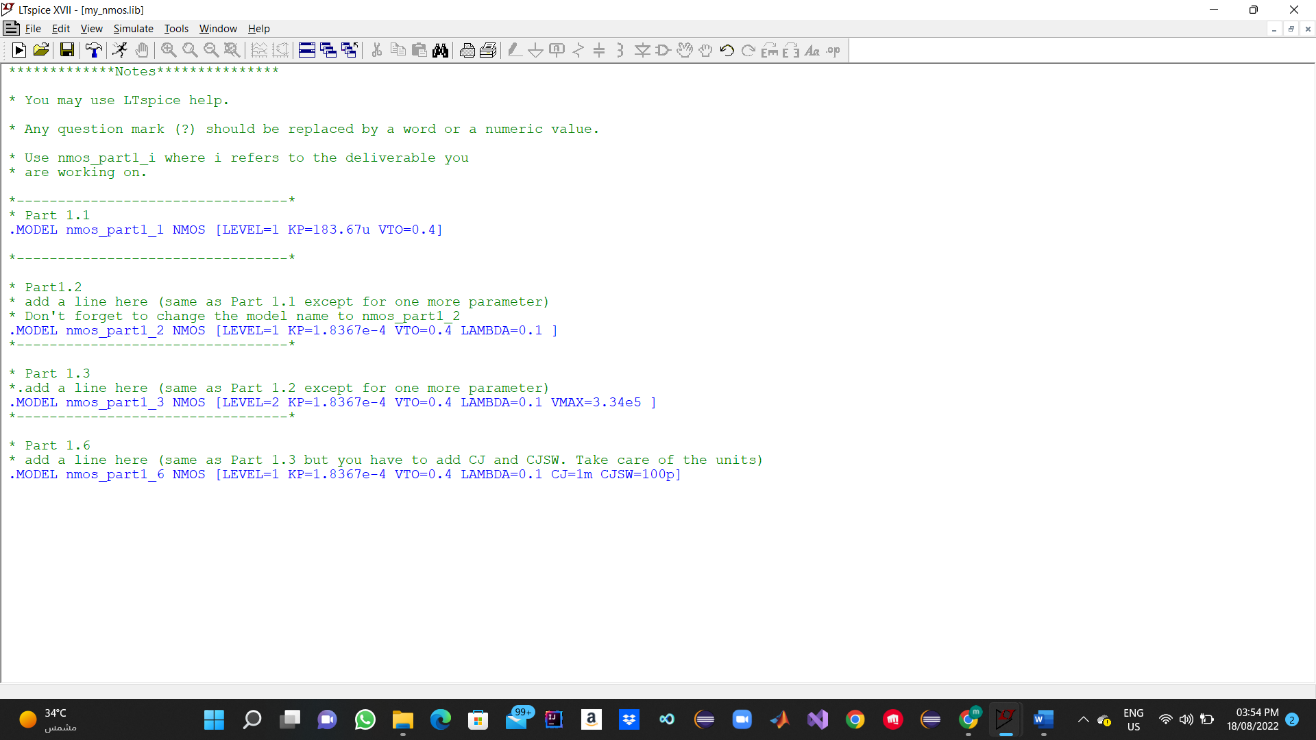
A screenshot of a computer

Description automatically generated

**Pmos Library :**

Graphical user interface, text, application, email

Description automatically generated

**Nmos Library :** 

Question 5:

Transient Graph :

**Graphical user interface, text

Description automatically generated**

Netlist: **Graphical user interface, text, application

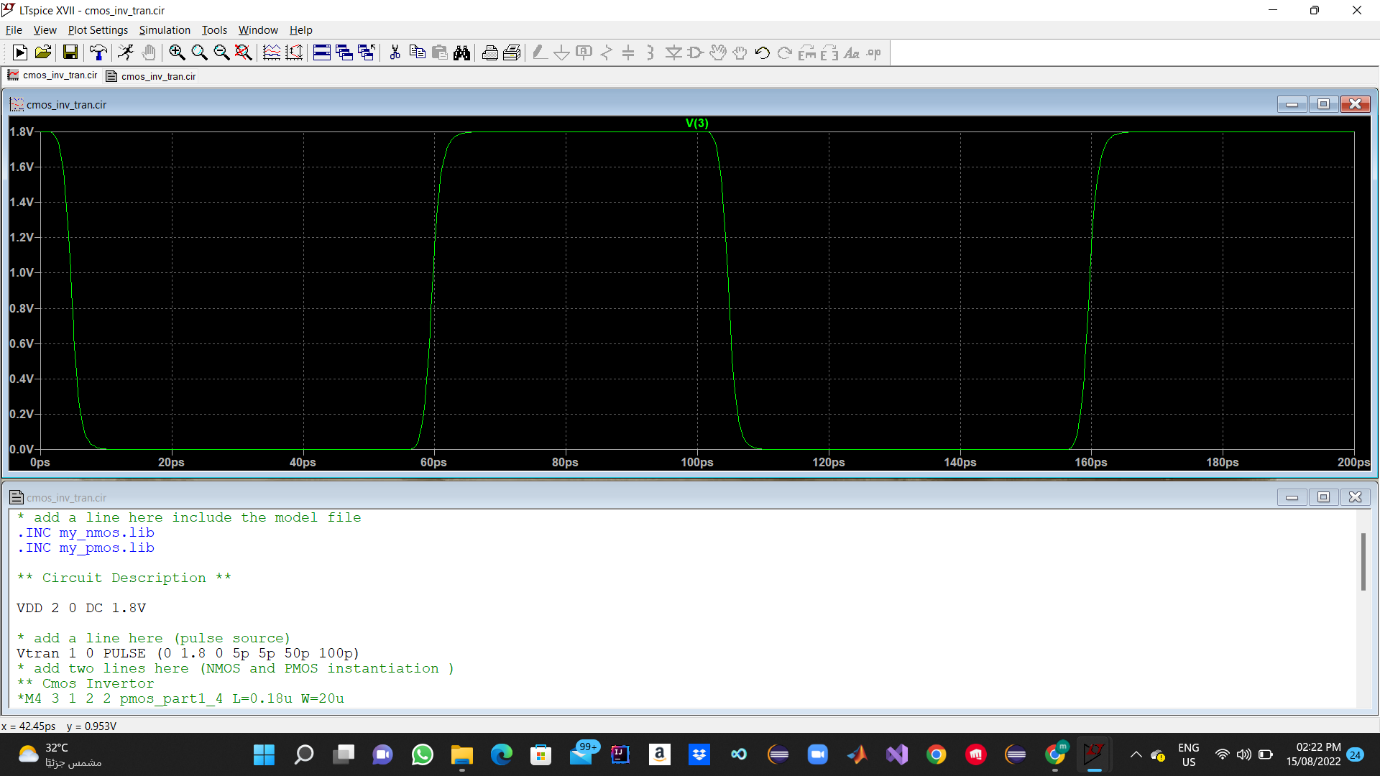
Description automatically generated**

**Delay Measurment: Graphical user interface, text

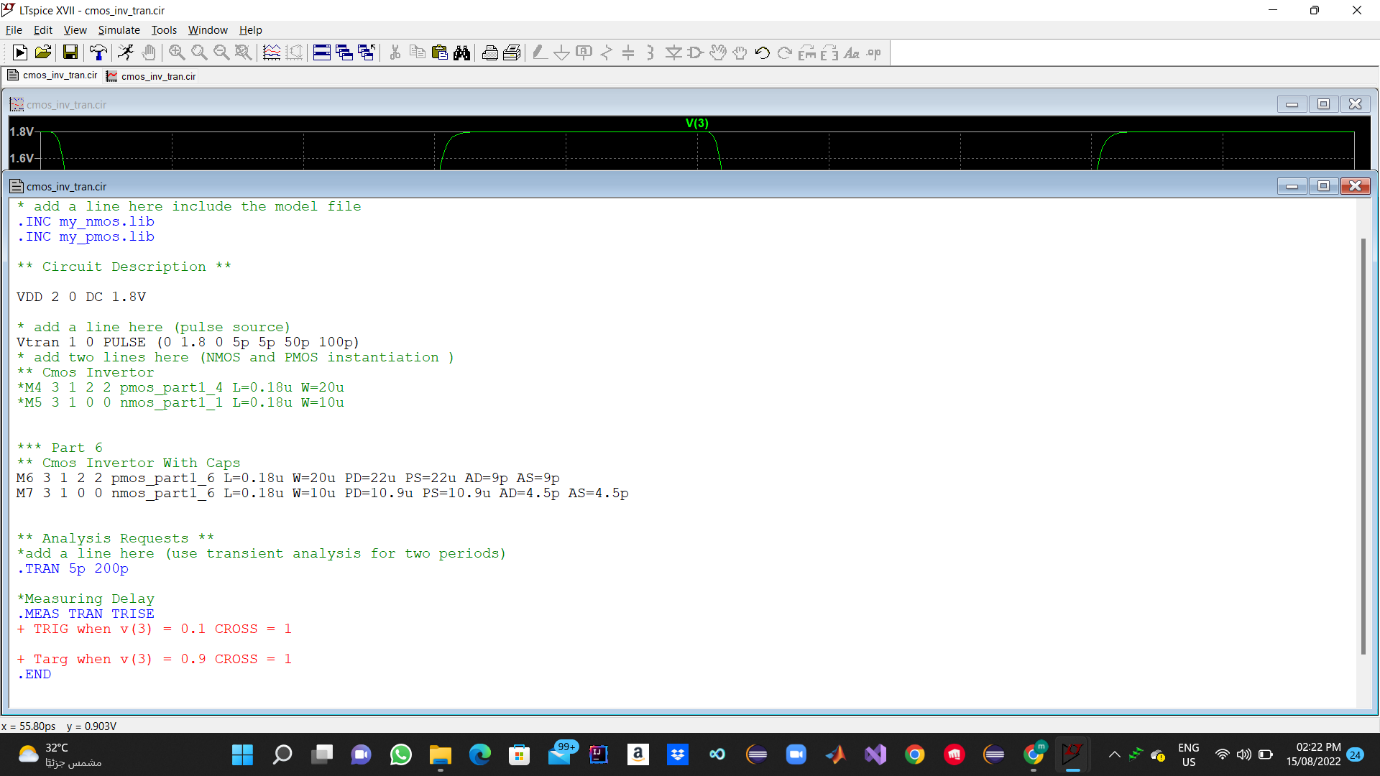
Description automatically generated**

Question 6:

Transient Graph :



Netlist:



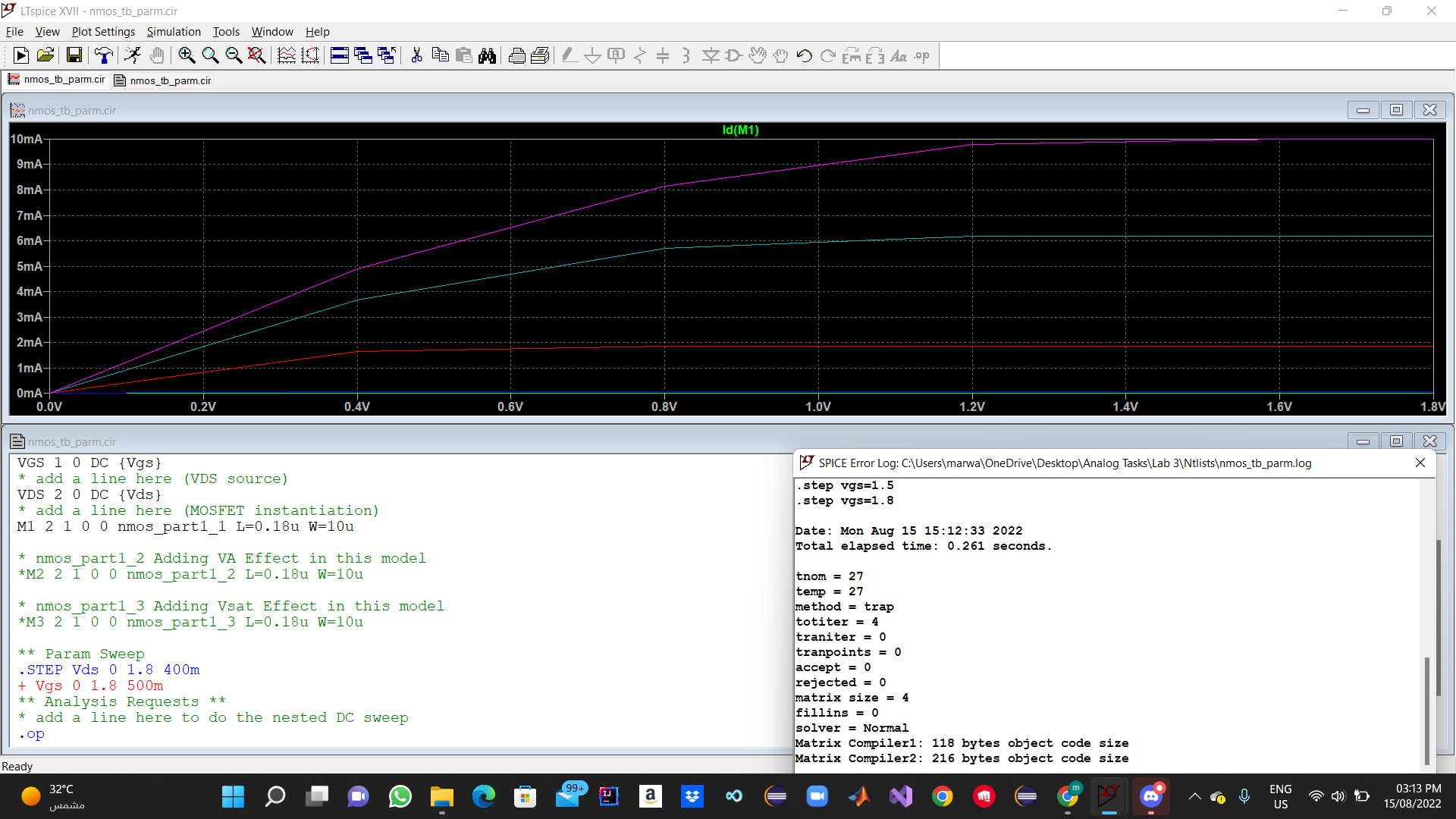
**Delay Measurment:**

Graphical user interface

Description automatically generated

PART2:

Question 1 :



Using Dc Sweep is much faster about 8.5x Faster Than using Parametric Sweeps.

Question 2 :

The files uses BSIM3v3 the Level Parameter Must be Set to Level 8 @Ltspice.

Graphical user interface, text

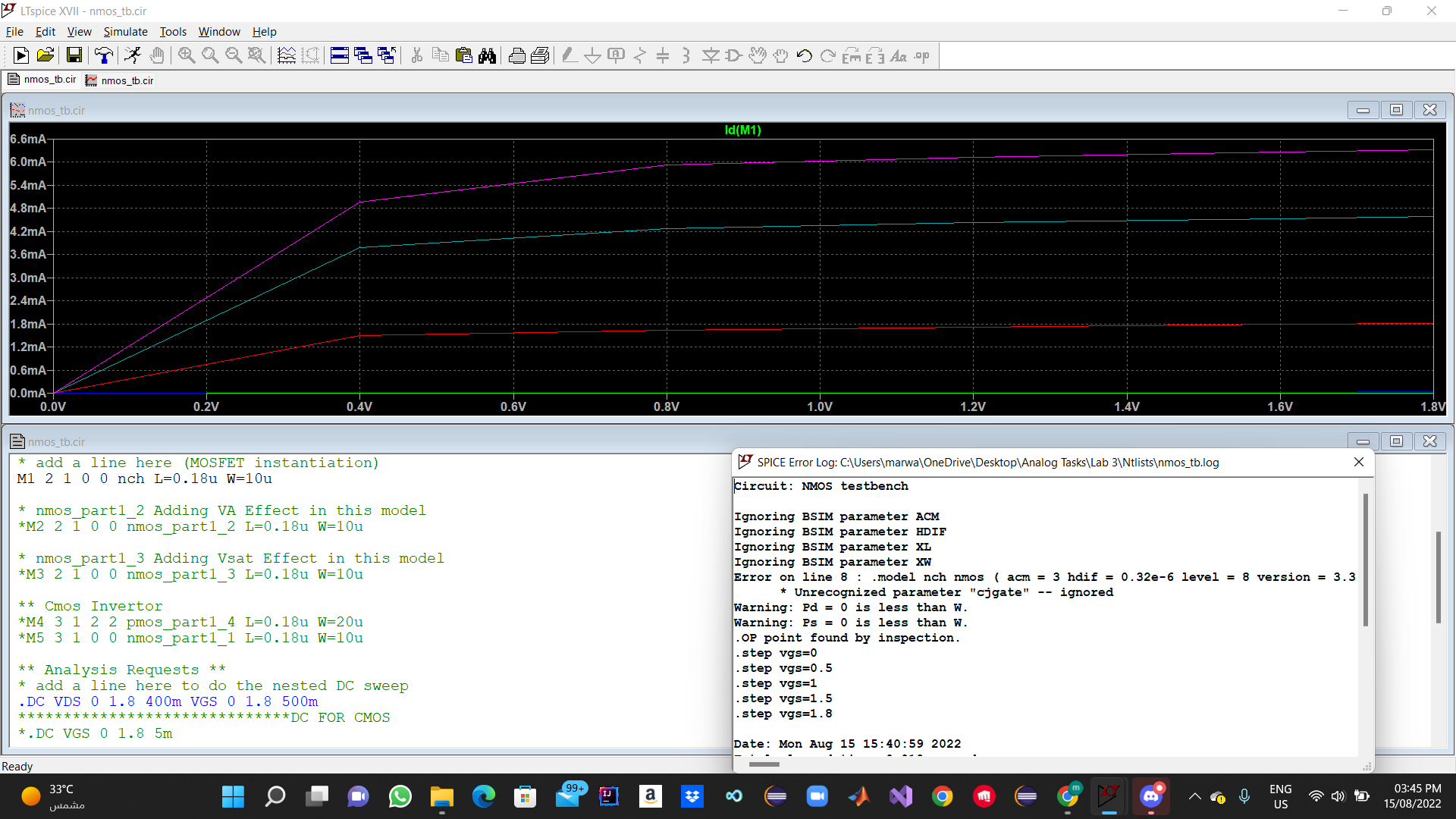
Description automatically generated

Level 1 Model :

Graphical user interface

Description automatically generated  
Bsim3v3 is more Accurate as it uses more Advanced Models , But Level 1 Uses The Square law which is valid only With Long Channel devices so it didn’t give accurate results for our 180n L Device As Shown.

Question 3 :



|  |  |
| --- | --- |
| ACM | Area Calculation Method it Describe How to Calculate the area of Drain , Source  Changing This will change in The Area of the Device and Capacitance. |
| HDIF | Length of highly Dopped Diffusion , will change The Capacitance of Source , Drain. |
| XL | Length for The Masking and Etching Process , It will Effect The Effective length of the Device. |
| XW | Width for The Masking and Etching Process , It will Effect The Effective Width of the Device. |

This BSIM Parameters are not supported in ltspice , if it was supported the area modifications will effect the caps that effects the speed of the transistor , and effective width may Effect the current.

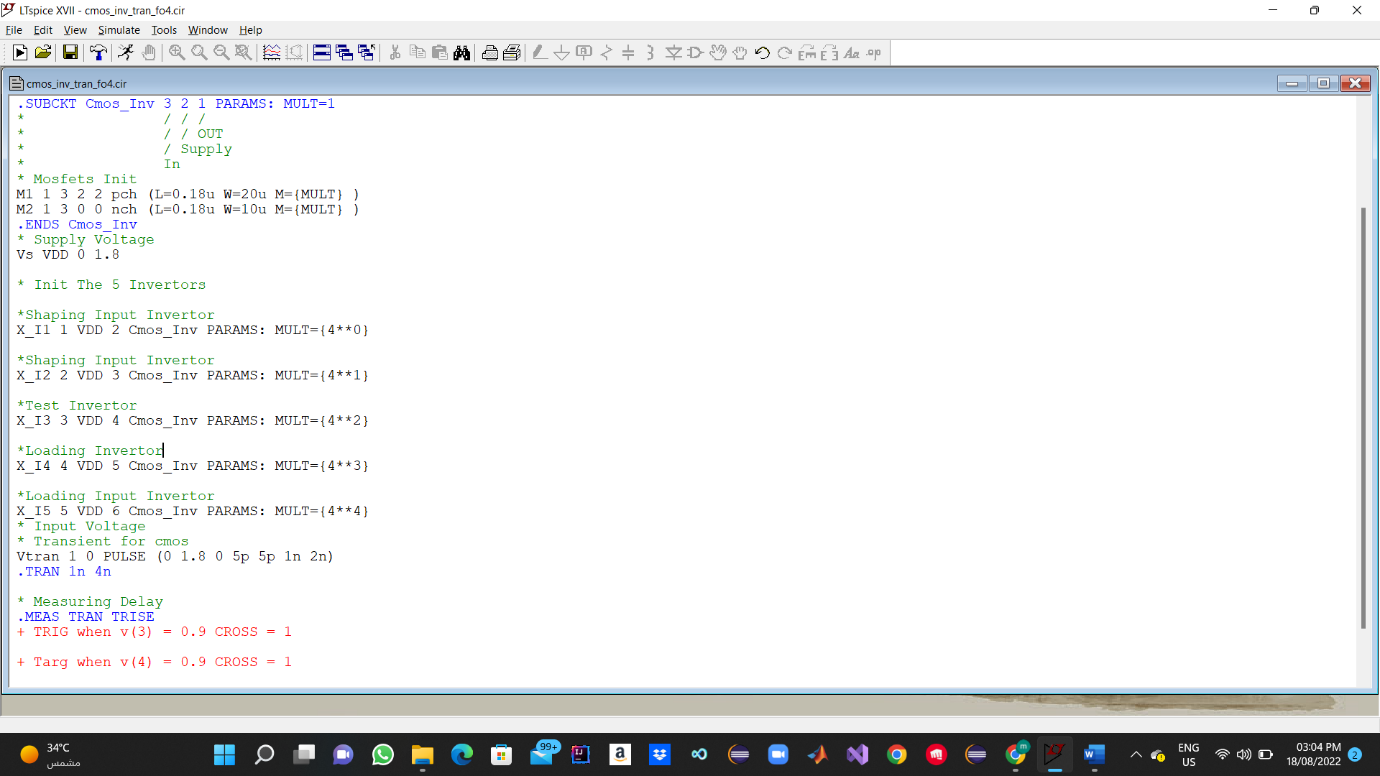
Question 4 :

FO4 Graph :

Graphical user interface

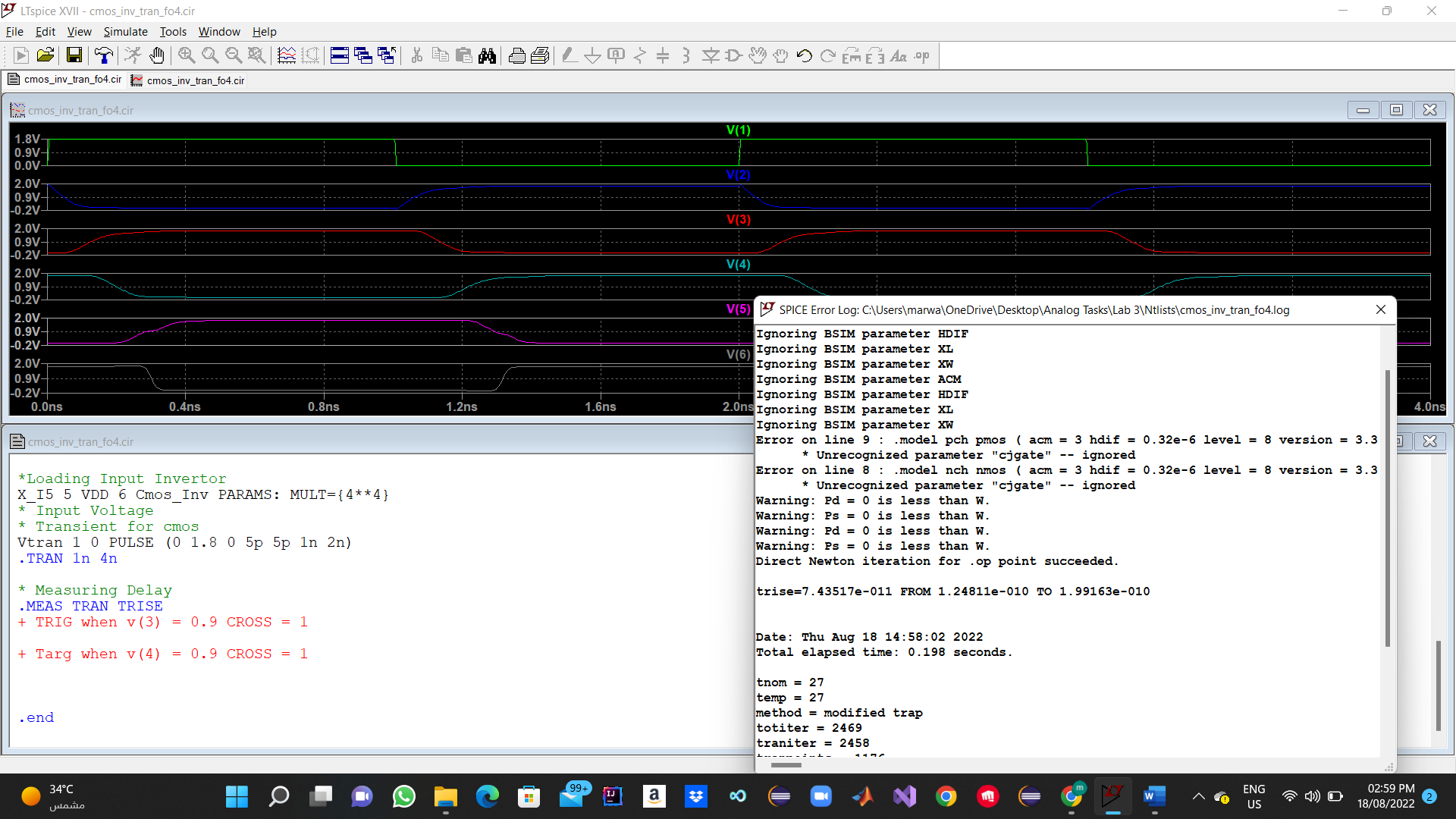
Description automatically generated with medium confidence

FO4 Netlist :



Question 5 :

Measuring Delay :



Delay/Lamda = 826.13E-6

Delay For 65nm Tech = 26.8492p